REMARKS

Claims 1-4 and 6-18, all the claims pending in the application, stand rejected on prior art grounds. Applicants respectfully traverse these rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1-2, 6-8 and 12-18 stand rejected under 35 U.S.C. §102(a) as being anticipated by Churchill (US Patent 6,392,941). Claims 3-4 and 9-10 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Churchill in view of Farnworth et al. (US Patent 5,994,915). Applicants respectfully traverse these rejections based on the following discussion.

A. The Rejection Based on Churchill

Churchill discloses a structure that includes a test line 102 connected to column select unit 140 and wordline select unit 142 that allows all word lines to be simultaneously selected, and does not teach or suggest the claimed common word lines common bit lines, common voltage lines, common ground lines, etc. that connect all the cells within a memory array as a single cell. In other words, Churchill merely discloses a test scheme that simultaneously activates all word lines to perform a stress test (column 1, lines 54-59) and does not teach or suggest the claimed common word lines common bit lines, common voltage lines, common ground lines, etc.

Paragraph 22 and 23 of Applicants' disclosure explains that the invention wires together all cells within the array to allow the cells to be testable as if they were a single cell. More specifically, within the array, all bit lines, word lines, N-wells, interior grounds, and interior voltages are wired in common to enable the array to be characterized for different components of leakage. As shown in Figure 1, the N-wells 105-108 are connected to a common N-well line 127 by connecting lines 125, 126. Similarly, bit line complement lines 120, 121 are connected to a

common bit line complement line 124 by connecting lines 122, 123. Also, the bit lines 115, 116 are connected to a common bit line 119 by connecting lines 117, 118. Further, word lines 110, 111 are connected to a common word line 112. Each of the cells 100-103 includes an interior ground component (GND) and an interior voltage component (VDD). The ground component is connected to a common interior ground line 132 by connecting lines 130, 131; and the interior voltage component is connected to a common interior voltage line 137 by connecting lines 135, 136. In addition, the invention includes a ground line 140 connected to the substrate.

This structure is clearly defined in the claims, where claim 1 defines "wherein said conductive lines: join all word lines within said array as a single word line; join all bit lines within said array as a single bitline; join all voltage lines within said array as a single voltage line; and join all ground lines together within said array as a single ground line." Similarly, independent claim 8 defines "a common word line; a common bit line; a common bit line complement line; a common N-well voltage line; a common interior ground line; a common interior voltage line; and a common ground line." In method form claim 14 defines " joining: all word lines within said array as a single word line; all bit lines within said array as a single bitline; all voltage lines within said array as a single voltage line; and all ground lines together within said array as a single ground line."

To the contrary, Churchill merely discloses a method that can stress all wordlines and bitlines in a SRAM simultaneously without causing damage due to excessive current, stress wordline and bitline features with a static supply voltage while having zero on-chip current, stress the wordline features of single wordline (SWL), double wordline (DWL) and/or other memory cell layouts, simultaneously apply an elevated supply voltage stress across the entire SRAM array multiple cell features, detect defects at sort that may cause post burn-in and/or post life stress failure, replace conventional high supply voltage functional testing with a much more stressful test, stress test bitlines/bitline bars, and/or apply all combinations of Vcc to Vss stresses (col 1, line 60-col 2, line 11).

The invention uses the foregoing connections to allow the entire array to be evaluated as a single cell. Therefore, for example, a charge can be placed upon any of the common lines while

the other lines are observed to determine whether current leakage occurs within any of the cells within the array. While no individual cell can be addressed uniquely, there are several important elements that can be learned. One is the lowest array leakage value, from the natural unwritten state. Another is the leakage variation with all cells written as a one and the leakage delta with all cells written as a zero (see Applicants' paragraph 28).

Thus, as shown above, Churchill does not teach or suggest the structure that is shown in Applicants' Figure 1 and defined by independent claims 1, 8, and 14. More specifically, Churchill does not teach or suggest "wherein said conductive lines: join all word lines within said array as a single word line; join all bit lines within said array as a single bitline; join all voltage lines within said array as a single voltage line; and join all ground lines together within said array as a single ground line" as defined by independent claim 1, "a common word line; a common bit line; a common bit line complement line; a common N-well voltage line; a common interior ground line; a common interior voltage line; and a common ground line", as defined by independent claim 8, or " joining: all word lines within said array as a single word line; all bit lines within said array as a single bitline; all voltage lines within said array as a single voltage line; and all ground lines together within said array as a single ground line" as defined by independent claim 14. Therefore, it is Applicants position that independent claims 1, 8, and 14 are patentable over Churchill. Further, dependent claims 2, 6, 7, 12, 13, and 15-18 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

B. The Rejection Based on Churchill in view of Farnworth et al.

The Office Action makes reference to Farnworth for the limited purpose of teaching a contact pad in rejecting dependent claims 3, 4, 9, and 10. However, while Farnworth does disclose the use of a contact pad, it does not teach or suggest that such pads are used in conjunction with the common word line, common bit line, common voltage line, common

ground line, etc. to allow the entire array to be tested as if it were a single cell as defined by dependent claims 3, 4, 9, and 10. Therefore, other than disclosing that contact pads have been used, Farnworth is otherwise irrelevant to the claimed invention and does not cure the deficiencies of Churchill that are discussed above. Therefore, it is Applicants position that dependent claims 3, 4, 9, and 10 are patentable, not only by virtue of their dependency from patentable independent claims 1 and 8, but also by virtue of the additional features of the invention they define. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

II. Formal Matters and Conclusion

Applicants submit that claims 1-4 and 6-18, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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